<u>PATENT</u>

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

1   Claim 1. (currently amended) A method of operating a programmable logic

2   integrated circuit comprising:

3   loading an initial value in a count register that is a part of a watchdog timer circuit

4   ~~on~~ <u>integrated as part of a</u> ~~the~~ programmable logic integrated circuit <u>disposed on a single die</u>;

5   clocking the count register to advance the count register to a next value with each

6   clock;

7   periodically reloading the count register with the initial value<u>, wherein the</u>

8   <u>reloading is caused by receiving a first magic value that configures the watchdog timer circuit to</u>

9   <u>respond to a second magic value that is different from the first magic value, wherein after</u>

10   <u>receiving the first magic value, upon receiving the second magic value, resetting the watchdog</u>

11   <u>timer circuit to the initial value</u>;

12   when the stored count value held in the count register that is a part of the

13   watchdog timer circuit reaches a final value, asserting a triggered signal output; and

14   upon receiving the triggered signal output in a reset logic block on the

15   programmable logic integrated circuit, causing reloading of configuration data from an external

16   source into the programmable logic integrated circuit.

1   Claim 2. (original) The method of claim 1 wherein the external source is a

2   nonvolatile memory.

1   Claim 3. (original) The method of claim 1 wherein the external source is a serial

2   EPROM.

1   Claim 4. (previously presented) The method of claim 1 wherein the final value

2   causes an overflow condition for the count register that is a part of the watchdog timer circuit.

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1   Claim 5. (original) The method of claim 1 wherein the watchdog timer circuit

2   increments the stored count value at each clock pulse.

1   Claim 6. (original) The method of claim 1 wherein the watchdog timer circuit

2   decrements the stored count value at each clock pulse.

1   Claim 7. (currently amended) The method of claim 1 wherein periodically

2   reloading the count register comprises:

3   writing a the first magic value into a reload register that is a part of the watchdog

4   timer circuit; and

5   when the first magic value is received in the reload register, resetting the count

6   register that is a part of the watchdog timer circuit to the initial value.

1   Claims 8. – 9. (canceled)

1   Claim 10. (previously presented) The method of claim 1 further comprising:

2   using the configuration data to configure an embedded processor portion and a

3   programmable logic portion on the programmable logic integrated circuit.

1   Claim 11. (original) The method of claim 1 wherein to avoid asserting the

2   triggered signal output, a periodic reload of the watchdog timer circuit should be performed

3   during a time period it takes the watchdog timer circuit to count from the initial value to the final

4   value.

1   Claim 12. (original) The method of claim 11 wherein the period is less than about

2   two minutes.

1   Claim 13. (original) The method of claim 11 wherein the time period depends or

2   clock frequency used to clock the watchdog timer circuit.

1   Claim 14. (original) The method of claim 1 wherein the initial value is 0 and the

2   final value is a maximum count value permitted by the count register.

1   Claim 15. (original) The method of claim 1 wherein the count register comprises

2   32 bits.

1   Claims 16. - 43. (cancelled).

1   Claim 44. (currently amended) A method of operating a programmable logic

2   integrated circuit comprising:

3   clocking a watchdog timer circuit on the programmable logic integrated circuit to

4   advance a count register that is a part of the watchdog timer circuit, wherein the programmable

5   logic integrated circuit and the watchdog timer circuit are disposed on the same die;

6   loading a first magic value into a reload register that is a part of the watchdog

7   timer circuit, which resets the count register to an initial value, wherein the first magic value

8   configures the watchdog timer circuit to respond to a second magic value that is different from

9   the first magic value;

10   after loading the first magic value, loading a the second magic value into the

11   reload register, which causes the count register to reset the initial value;

12   after loading the first magic value into the reload register, loading a value other

13   than the second magic value into the reload register, which causes the watchdog timer circuit to

14   generate a triggered signal; and

15   receiving the triggered signal in a reset logic block on the programmable logic

16   integrated circuit, which causes a reloading of configuration data from an external source into the

17   programmable logic integrated circuit.

1   Claim 45. (cancelled)

1   Claim 46. (previously presented) The method of claim 44 wherein the

2   configuration data is used to configure an embedded processor portion and a programmable logic

3   portion on the programmable logic integrated circuit.

1   Claim 47. (previously presented) The method of claim 44 wherein the watchdog

2   timer circuit is located in an embedded processor portion and the reset logic block is located in a

3   programmable logic portion on the programmable logic integrated circuit.

1   Claim 48. (previously presented) The method of claim 44 further comprising:

2   allowing the count register that is a part of the watchdog timer circuit to advance

3   to a final value before the first or second magic values are loaded, which causes the watchdog

4   timer circuit to generate the triggered signal.

1   Claim 49. (original) The method of claim 44 wherein the initial value is 0.

1   Claim 50. (original) The method of claim 44 wherein the initial value is a value

2   other than 0.

1   Claim 51. (currently amended) The method of claim 44 wherein the ~~first magic~~

2   ~~value is different from the~~ second magic value <u>configures the watchdog timer circuit to respond</u>

3   <u>to a third magic value that is different from the second magic value</u>.

1   Claim 52. (original) The method of claim 48 wherein the final value is user-

2   selectable.

1   Claim 53. (original) The method of claim 48 wherein the final value is the

2   maximum count permitted by the count register.

1   Claim 54. (original) The method of claim 44 wherein in a debug mode, the count

2   register does not advance.